SELECTABLE MEMORY WORD LINE DEACTIVATION

Background of the Invention

[0001] This invention relates to integrated circuit memories. More particularly, this invention relates to the deactivation of selected word lines in dynamic random access memories (DRAMs).

[0002] A DRAM is a form of semiconductor random access memory (RAM) commonly used as main memory in computers and other electronic systems. DRAMs store information in integrated circuits called cells, which hold one bit of information each. Cells are typically grouped into one-dimensional arrays called words.

[0003] In certain DRAM architectures, selection of a word for reading or writing occurs as follows: the word to be activated is determined by decoding an address. The selected word line (WL) is then connected to a common node with a sufficiently positive voltage, typically referred to as the VCCP node. Similarly, deactivation involves connecting the WL to a common node with a negative or sufficiently low voltage. This node may be ground or a special purpose node referred to herein as VWLN. As transistor sizes continue to shrink and transistor leakage current becomes more of a problem, the VWLN node is preferred over ground.

[0004] More than one WL may be activated or deactivated simultaneously for testing or other purposes. A problem sometimes arises when deactivating multiple WLs. The positive electrical charge residing on a previously activated word line discharges into the VWLN node, pulling the node's voltage up. In some cases, VWLN node voltage may increase enough to inadvertently activate WLs intended to remain deactivated, thus adversely affecting data integrity throughout a system.

[0005] Many systems rely on a single pre-charge signal that is shared across all WLs for WL deactivation. This sharing forces all WLs to be deactivated simultaneously. As a result, it is often impractical to activate more than a few WLs at a time, because their simultaneous deactivation could cause a substantial change in VWLN node voltage.

[0006] In view of the foregoing, it would be desirable to provide circuitry and methods that reduce the voltage fluctuation at the VWLN node, thus allowing more WLs to be active at the same time.

Summary of the Invention

[0007] It is an object of this invention to provide circuitry and methods that reduce the voltage fluctuation at the VWLN node, thus allowing more WLs to be active at the same time.

[0008] In accordance with this invention, circuitry and methods are provided that deactivate selected WLs individually or in small selectable numbers, substantially reducing voltage fluctuation at the VWLN node. All activated WLs can still be deactivated in a short period of time, but their cumulative effect on VWLN node voltage is reduced, because the deactivation of all WLs is no longer simultaneous. That is, the number of simultaneously deactivated WLs can be controlled.

[0009] In a preferred embodiment of the invention, each WL is activated and deactivated by the output of a respective row address latch circuit. The latch circuit's inputs include an ACTIVE signal shared by all WLs and an address bit specific to each WL. By pulsing the ACTIVE signal while the address bit is active, a specific WL's activation status (i.e., active or inactive) can be toggled. This allows selected WLs to be deactivated, advantageously avoiding the simultaneous deactivation of all active WLs.

[0010] The invention therefore advantageously reduces voltage fluctuation at the VWLN node when deactivating multiple WLs, thus permitting more WLs to be active concurrently. This is particularly useful in reducing test time.

Brief Description of the Drawings

[0011] The above and other objects and advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

[0012] FIG. 1 is a circuit diagram of typical DRAM cells;

[0013] FIG. 2 is a block diagram of a representative WL activation/deactivation architecture;

[0014] FIG. 3 is a circuit diagram of a typical row address latch;

[0015] FIG. 4 is a timing diagram of input and output signals of the row address latch of FIG. 3;

[0016] FIG. 5 is a circuit diagram of an exemplary embodiment of a row address latch according to the invention;

[0017] FIG. 6 is a timing diagram of input and output signals of the row address latch of FIG. 5 according to the invention;

[0018] FIG. 7 is a block diagram of an alternative WL activation/deactivation architecture that incorporates the invention; and

[0019] FIG. 8 is a block diagram of a system that incorporates the invention.

Detailed Description of the Invention

[0020] DRAMs are, in their simplest form, arrays of cells each including a capacitor for holding a charge and a transistor acting as a switch for accessing the charge held in the capacitor. DRAM arrays are typically arranged in columns and rows. FIG. 1 shows four DRAM cells 102a,b,c,d (four cells are shown merely for illustrative purposes). Each row of cells 104a and 104b is called a word. The transistor of each cell in a word is connected to a shared WL 106a or 106b. WLs 106a and 106b control the ON/OFF state of transistors 108a,b,c,d, which allow information to be read from or written to capacitors 110a,b,c,d. The information to be read or written is transferred via bit lines 112a,b. When a WL is activated, it drives the coupled transistors conductive (i.e., turns the transistors ON).

[0021] FIG. 2 shows a representative activation/deactivation architecture for a DRAM with four WLs. The two-bit ADDRESS signal specifying which WL to activate is input into an address decoder 202. Decoder 202 has one output for each WL. It determines which WL is specified by the address and activates the corresponding output. The address decoder's outputs are then processed by row address latches 204. Each row address latch has three inputs, the ADDR signal from the decoder, a shared ACTIVE signal, and a shared PRE-CHARGE signal. Each row address latch has one output, which is connected to a specific WL. For example, the top row address latch has output signal W0, which is connected to WL0. The PRE-CHARGE signal

deactivates all WLs in a section of a DRAM chip by connecting them to the VWLN node. The ACTIVE signal is pulsed after the address decoder's outputs have settled in order to activate only the target WL. During the pulse, each row address latch activates its output W and connects the WL to the VCCP node if its ADDR signal is active. After a WL has been activated, it can ordinarily only be deactivated by asserting the PRE-CHARGE signal.

[0022] FIG. 3 shows a typical row address latch 300. Latch 300 includes p-type transistor 302, n-type transistors 304 and 306, and inverters 308, 310, 312, and 314. Node 301 can be coupled to VCCP or another voltage level. Inputs PRE-CHARGE and ADDR0 are active low (i.e., activated by a logical 0 signal), while ACTIVE is active high (i.e., activated by a logical 1 signal). When PRE-CHARGE is driven to a logical 0, it activates transistor 302, which drives W0 low. Note that after PRE-CHARGE is asserted low, transistor 306 becomes conductive.

[0023] When the ACTIVE signal is a high pulse, it drives transistor 304 conductive. During the pulse, if ADDR0 is active (i.e., low), it drives output W0 high and activates the corresponding WL. When W0 is high, transistor 306 is non-conductive (its input from inverter 312 is low), and subsequent pulses on the ACTIVE input will have no effect on the W0 output. To deactivate this WL, the PRE-CHARGE signal is asserted low, which also simultaneously deactivates all other WLs in the same section of the DRAM chip. As described above, this can have an adverse effect on other WLs depending on the number of WLs being simultaneously deactivated.

[0024] FIG. 4 shows a timing diagram 400 in which three row address latches of FIG. 3 are used to respectively activate and deactivate three WLs. Signal CLK is a system clock signal. When PRE-CHARGE is

pulsed low at signal transition 402, all three WLs are deactivated. Signal ACTIVE is then pulsed three times in conjunction with signal ADDRESS at signal transitions 403-405, activating W0, W1, and W2 in turn. Finally, when signal PRE-CHARGE is again pulsed low at signal transition 406, all three WLs are simultaneously deactivated in transition 408, causing the three associated WLs to be connected to the VWLN node. This simultaneous deactivation can result in a substantial amount of positive charge flowing into the VWLN node, causing the node's voltage to drift upwards undesirably.

[0025] An exemplary embodiment of the invention is shown in FIG. 5. Row address latch circuit 500 includes p-type transistors 502 and 516, n-type transistors 504 and 506, inverters 508, 510, 512, and 514, delay element 518, and logic 520. Nodes 501 can be coupled to VCCP or another voltage level. Logic 520 controls transistor 516 via signal DEAC and preferably includes NOR gate 522 and inverters 524, 526, and 528. The SWLD input signal is active high and enables latch circuit 500 to selectively deactivate its WL.

[0026] Circuit 500 responds to a PRE-CHARGE pulse by deactivating its output W0 in the same fashion as latch circuit 300. When the ACTIVE signal is pulsed high while signal ADDR0 is low, output W0 will be asserted high. Note that during this assertion phase, transistor 516 is non-conductive, because the DEAC signal is a logical 1 when the ACTIVE pulse arrives. When ACTIVE is again pulsed high while SWLD is high and ADDR0 is low, logic 520 outputs the DEAC signal low, driving transistor 516 conductive and de-asserting W0. Thus, the row address latch according to the invention allows a specific WL to be deactivated, without using the PRE-CHARGE signal which is shared across all WLs. Delay element 508 assures that the ACTIVE pulse passes before output signal OPEN becomes high, driving

transistor 506 conductive (signal OPEN is also fed to NOR gate 522). Note that until the next pulse of the PRE-CHARGE signal resets latch circuit 500, each time ACTIVE is pulsed high while SWLD is high and ADDR0 is low, the value of W0 will toggle (i.e., alternate between a logical 1 and a logical 0).

[0027] FIG. 6 shows a timing diagram 600 of signals applied to latch circuit 500 according to the invention. Similar to latch circuit 300, transition 602 of signal PRE-CHARGE deactivates all WLs. Following this deactivation, the ACTIVE signal is pulsed three times in transitions 603-605 to activate all three WLs. Advantageously, however, the WLs can each be deactivated without asserting the PRE-CHARGE signal, and the deactivation of each WL need not be simultaneous with the deactivation of other WLs. Rather, the three successive pulses of the ACTIVE signal shown in transitions 606a, 607a, and 608a deactivate the three WLs in turn, illustrated in transitions 606b, 607b, and 608b. This non-simultaneous deactivation results in smaller transient spikes on the VWLN node than that caused by the simultaneous deactivation of all WLs at transition 408 of timing diagram 400.

[0028] Note that circuit 500 and timing diagram 600 are both merely illustrative. Other latch circuits that toggle the W0 output independently of the PRE-CHARGE signal can be used. For example, p-channel field effect transistor 516 could be replaced with an n-channel field effect transistor if inverter 528 were removed. Similarly, if the PRE-CHARGE signal were active high, transistor 502 could be replaced with an n-channel field effect transistor. Another possibility would be to force the output W0 to swing between ground and VCCP, rather than between VWLN and VCCP, by setting the voltage range of inverter 514 appropriately.

[0029] Also, the number of row address latches controlling each WL can vary from that shown. For example, FIG. 7 shows an activation/deactivation architecture where each WL is controlled by two row address latches. Architecture 700 includes address pre-decoders 702, row address latches 500, row address latches 300, and logical AND gates 706. In this example, decoding of a four-bit address occurs in two stages. In the first stage, the address' two most significant bits ADDRESS_MSB and its two least significant bits ADDRESS_LSB are separately decoded. Each address pre-decoder 702 outputs one ADDR signal low, and the others high. These outputs are then processed by row address latches 500 or 300 according to the invention. In the final stage of decoding, each WL is tied to the outputs of two row address latches by an AND gate 706, one latch output for each address pre-decoder 702. These two latch outputs represent the combination of ADDRESS_MSB and ADDRESS_LSB values that correspond to a particular WL's address. Thus, a given WL can only be activated if both its corresponding latch outputs are high. Note that, in FIG. 7, any given row address latch 500 is tied to more than one WL. Thus, in contrast with the architecture of FIG. 2, the architecture shown in FIG. 7 makes it possible to activate or deactivate multiple WLs with a single ACTIVE pulse. For instance, suppose the four WLs tied to signals W0-W3 were activated. If latch output RA0 were subsequently driven low, then those four WLs would all be simultaneously deactivated. The number of row address latches could alternatively depend on other considerations as well.

[0030] Timing diagram 600 could also vary, depending on the particular application required. For example, circuit 500 could be used to deactivate only WL0 and WL1, and the PRE-CHARGE signal could have been pulsed to deactivate WL2. Other operation sequences are

possible, depending on, for example, the task to be performed and the limitations of the hardware.

[0031] FIG. 8 shows a system that incorporates the invention. System 800 includes a plurality of DRAM chips 801, a processor 880, a memory controller 882, input devices 884, output devices 886, and optional storage devices 888. DRAM chips 801 each include one or more latch circuits 500. Data and control signals are transferred between processor 880 and memory controller 882 via bus 881. Similarly, data and control signals are transferred between memory controller 882 and DRAM chips 801 via bus 883. Input devices 884 can include, for example, a keyboard, a mouse, a touch-pad display screen, or any other appropriate device that allows a user to enter information into system 800. Output devices 886 can include, for example, a video display unit, a printer, or any other appropriate device capable of providing output data to a user. Note that input devices 884 and output devices 886 can alternatively be a single input/output device. Storage devices 888 can include, for example, one or more disk or tape drives.

[0032] Note that the invention is not limited to DRAM chips, but is applicable to other integrated circuit chips having a circuit or group of circuits where the simultaneous activation or deactivation of certain signal lines is undesirable.

[0033] Thus it is seen that circuits and methods are provided to deactivate multiple WLs individually or in small selectable numbers, thus reducing the total number of WLs deactivated simultaneously. One skilled in the art will appreciate that the invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.